

one of an emitter layer and a source layer of the first conductivity type selectively formed on the surface of said base layer of the second conductivity type;

one of a collector layer and a drain layer selectively formed on one of the one surface and another surface of said base layer of the first conductivity type;

a first main electrode formed on said one of said collector layer and said drain layer;

a second main electrode formed on said one of said emitter layer and said source layer and on said base layer of the second conductivity type; and

a gate electrode formed with first and second gate insulating films on said base layer of the second conductivity type that lies between said one of said emitter layer and said source layer and said base layer of the first conductivity type,

wherein a capacitance of a capacitor formed on the second gate insulating film is different from a capacitance of a capacitor formed on the first gate insulating film.

2. (Amended) The power semiconductor device according to claim 1, wherein the first gate insulating film is formed in a portion near said one of said emitter layer and said source layer, and the second gate insulating film is formed in a portion near said base layer of the first conductivity type.

3. (Amended) The power semiconductor device according to claim 2, wherein a thickness of the second gate insulating film is larger than a thickness of the first gate insulating film.

4. (Amended) The power semiconductor device according to claim 2, wherein a dielectric constant of the second gate insulating film is smaller than a dielectric constant of the first gate insulating film.

5. (Amended) The power semiconductor device according to claim 2, wherein a thickness of the second gate insulating film has an inclination and the thickness thereof on a side of said one of said emitter layer and said source layer is smaller than a thickness on a side of said base layer of the first conductivity type.

6. (Amended) The power semiconductor device according to claim 1, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from a surface of said one of said emitter layer and said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

7. (Amended) The power semiconductor device according to claim 2, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from a surface of said one of said emitter layer and said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

8. (Amended) The power semiconductor device according to claim 3, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from a surface of

said one of said emitter layer and said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

9. (Amended) The power semiconductor device according to claim 4, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from a surface of said one of said emitter layer and said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

10. (Amended) The power semiconductor device according to claim 5, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from a surface of said one of said emitter layer and said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

11. (Amended) A method of manufacturing a power semiconductor device comprising:

forming a base layer of a first conductivity type;

selectively forming a base layer of a second conductivity type on one surface of the base layer of the first conductivity type;

selectively forming one of an emitter layer and a source layer of the first conductivity type on a surface of the base layer of the second conductivity type;

selectively forming one of a collector layer and a drain layer on one of the one surface and another surface of the base layer of the first conductivity type;

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forming a first main electrode on said one of the collector layer and the drain layer;  
forming a second main electrode on said one of the emitter layer and the source layer  
of the first conductivity type and on the base layer of the second conductivity type; and  
forming first and second gate insulating films on the base layer of the second  
conductivity type that lies between said one of the emitter layer and the source layer of the  
first conductivity type and the base layer of the first conductivity type and forming a gate  
electrode on the first and second gate insulating films;  
wherein a capacitance of a capacitor formed on the second gate insulating film is  
different from a capacitance of a capacitor formed on the first gate insulating film.

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**Please add new Claims 12-20 as follows.**

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12. (New) The method of manufacturing a power semiconductor device according to  
claim 11, wherein the first gate insulating film is formed in a portion near said one of said  
emitter layer and source layer and the second gate insulating film is formed in a portion near  
said base layer of the first conductivity type.

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13. (New) The method of manufacturing a power semiconductor device according to  
claim 12, wherein a thickness of the second gate insulating film is larger than a thickness of  
the first gate insulating film.

14. (New) The method of manufacturing a power semiconductor device according to  
claim 12, wherein a dielectric constant of the second gate insulating film is smaller than a  
dielectric constant of the first gate insulating film.

15. (New) The method of manufacturing a power semiconductor device according to claim 12, wherein a thickness of the second gate insulating film has an inclination and the thickness thereof on a side of said one of said emitter layer and said source layer is smaller than a thickness on a side of said base layer of the first conductivity type.

16. (New) The method of manufacturing a power semiconductor device according to claim 11, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from a surface of said one of said emitter layer and said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

17. (New) The method of manufacturing a power semiconductor device according to claim 12, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from a surface of said one of said emitter layer and said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

18. (New) The method of manufacturing a power semiconductor device according to claim 13, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from a surface of said one of said emitter layer and said source layer to an intermediate

portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

19. (New) The method of manufacturing a power semiconductor device according to claim 14, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from a surface of said one of said emitter layer and said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

20. (New) The method of manufacturing a power semiconductor device according to claim 15, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from a surface of said one of said emitter layer and said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

#### REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-20 are presently active. Claims 1-11 have been amended; and Claims 12-20 have been added by the present amendment. The changes and additions to the claims are supported by the originally filed specification and do not add new matter.